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EP 0565127 A2 US 5175511 A US 4752749 A
US 4568888 A US 4330758 A

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INT CL[6] H03L , H04B , H04L
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(54) Frequency hopping in a TDMA system

(57) A method for implementing frequency hopping in a time domain system having at least a first synthesiser 42 including the steps of locking onto a first frequency by the first synthesiser in wide loop bandwidth mode, transmitting from the first synthesiser, and converting to a narrow bandwidth mode on the first synthesiser after a delayed period of time. The apparatus includes two frequency synthesisers 42, 40 frequency hopping on a time slot by time slot basis. While one synthesiser e.g. 42 is in a narrow bandwidth and transmitting, the other synthesiser is disconnected and being tuned to the next frequency. Switch over between synthesisers and ramping up in power takes place in the guard band between the slots. Applications may be in TDMA based cellular systems.

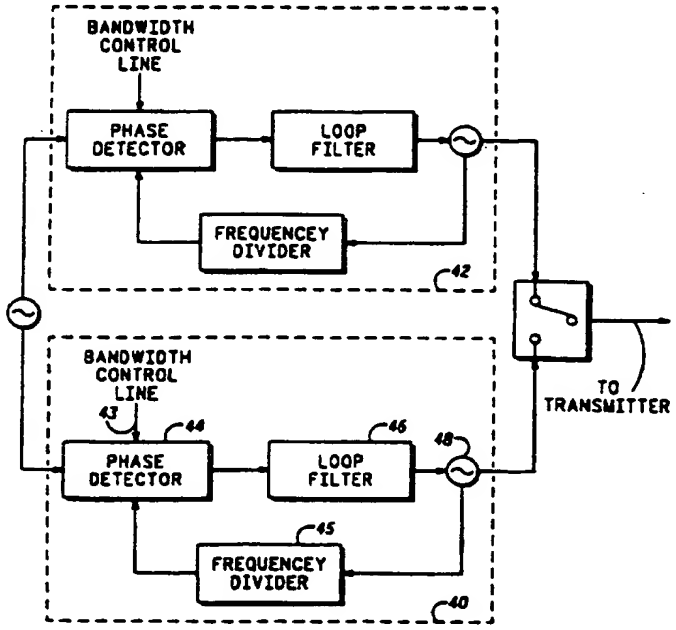

FIG. 4

GB 2 295 930 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

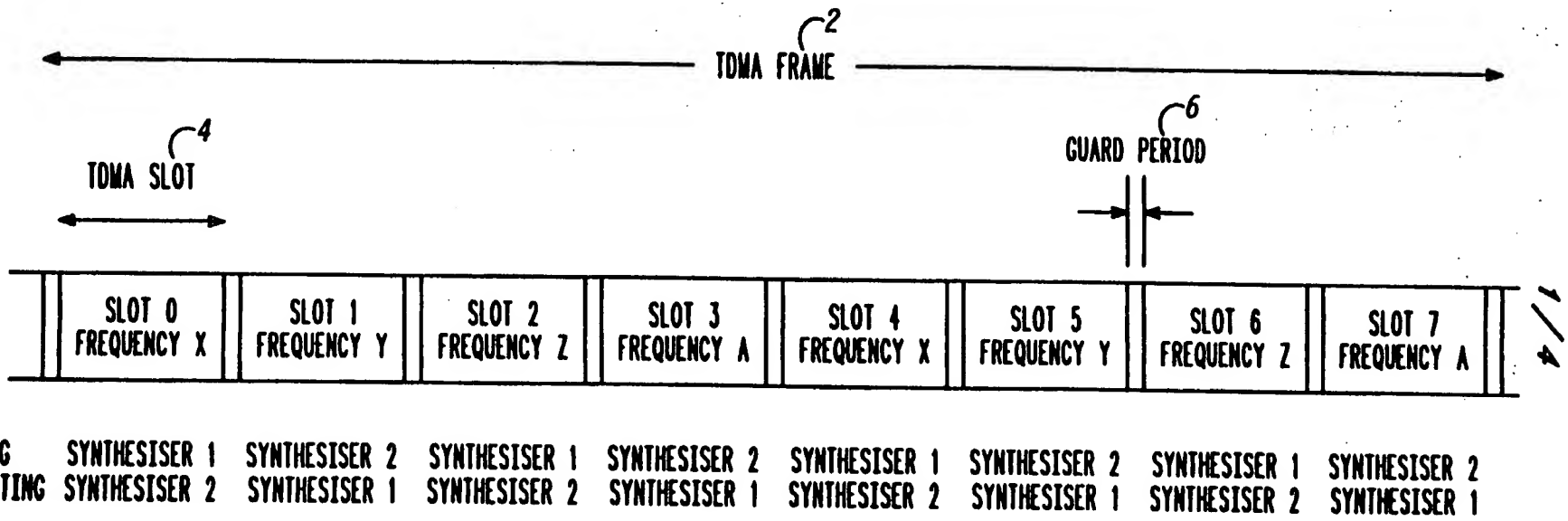
2
TDMA FRAME
4
TDMA SLOT
6
GUARD PERIOD
SLOT 0 FREQUENCY X
SLOT 1 FREQUENCY Y
SLOT 2 FREQUENCY Z
SLOT 3 FREQUENCY A
SLOT 4 FREQUENCY X
SLOT 5 FREQUENCY Y
SLOT 6 FREQUENCY Z
SLOT 7 FREQUENCY A
TUNING SYNTHESISER 1 SYNTHESISER 2 SYNTHESISER 1 SYNTHESISER 2 SYNTHESISER 1 SYNTHESISER 2 SYNTHESISER 1 SYNTHESISER 2
TRANSMITTING SYNTHESISER 2 SYNTHESISER 1 SYNTHESISER 2 SYNTHESISER 1 SYNTHESISER 2 SYNTHESISER 1 SYNTHESISER 2 SYNTHESISER 1

FIG. 1

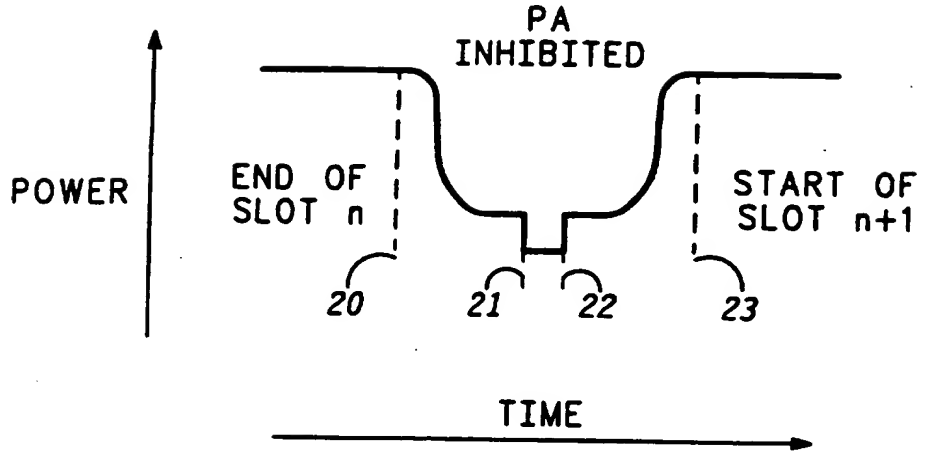
PA
INHIBITED
POWER
END OF
SLOT n
START OF
SLOT n+1
20
21
22
23
TIME

FIG. 2

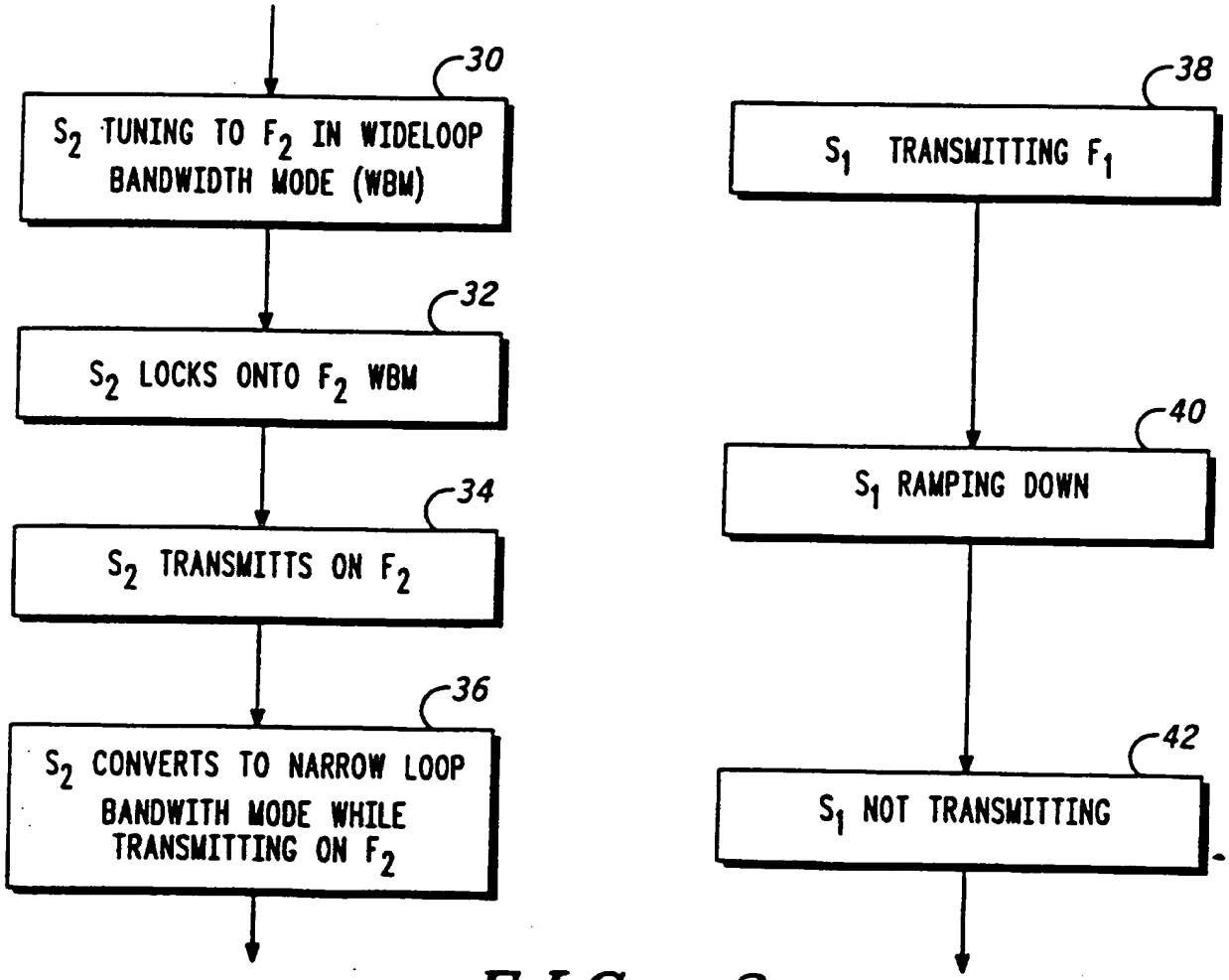
30
S_2 TUNING TO F_2 IN WIDELOOP BANDWIDTH MODE (WBM)
32
S_2 LOCKS ONTO F_2 WBM
34
S_2 TRANSMITTS ON F_2
36
S_2 CONVERTS TO NARROW LOOP BANDWITH MODE WHILE TRANSMITTING ON F_2
38
S_1 TRANSMITTING F_1
40
S_1 RAMPING DOWN
42
S_1 NOT TRANSMITTING

FIG. 3

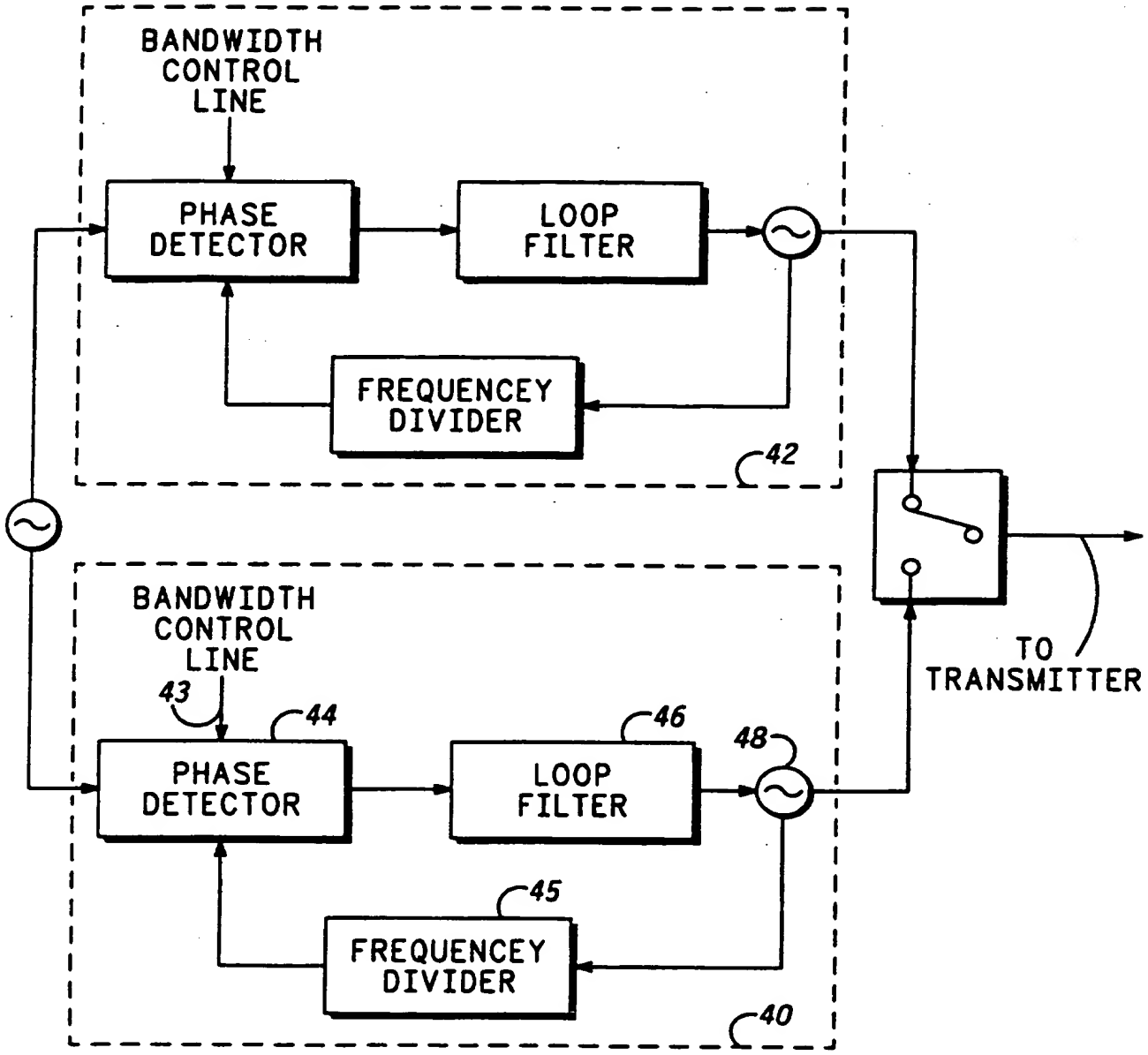
BANDWIDTH CONTROL LINE
PHASE DETECTOR
LOOP FILTER
FREQUENCEY DIVIDER
42
BANDWIDTH CONTROL LINE
43
44
PHASE DETECTOR
46
LOOP FILTER
48
45
FREQUENCEY DIVIDER
40
TO TRANSMITTER

FIG. 4

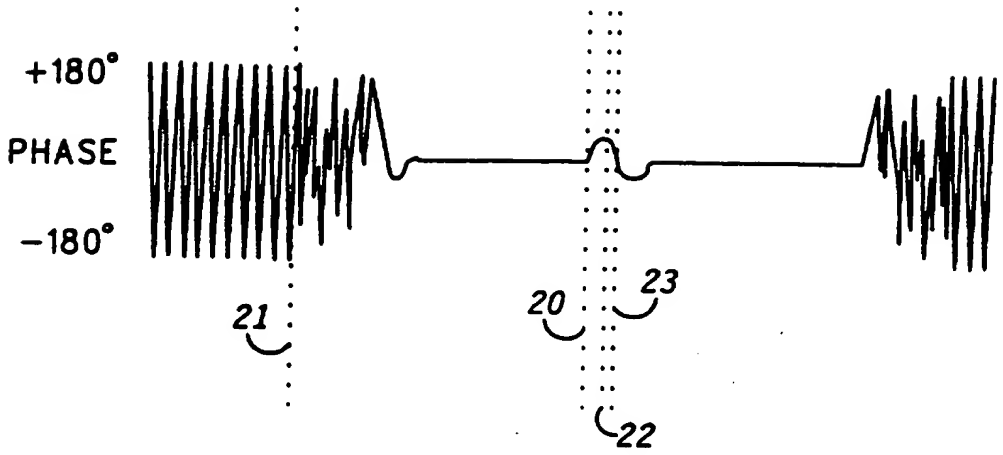

FIG. 5

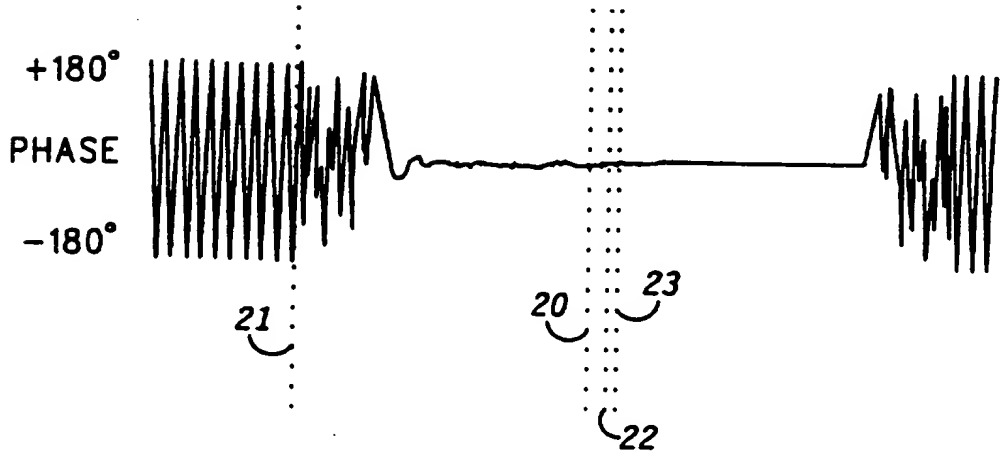

FIG. 6

METHOD AND APPARATUS FOR IMPLEMENTING FREQUENCY HOPPING IN A TDMA SYSTEM

Field of the Invention

This invention relates in general to communications systems, and more particularly to a method for implementing frequency hopping in a time domain system.

Background to the Invention

Base station transceivers for TDMA communications systems such as DCS1800, have to be capable of supporting frequency hopping on a time slot by time slot basis. This requirement influences the linearity of the transmitter since power ramping must be employed to reduce spurious emissions from the step changes in transmit frequency. In order to reduce side-lobe levels it is desirable to spread the power ramp over a wide period. As a result, the synthesiser has an extremely small window in which to hop. Several problems are encountered in the implementation of such a synthesiser, such as fast acquisition, low noise and high resistance to frequency pulling.

Slow frequency hopping is commonly employed in TDMA based cellular systems. In slow frequency hopping (SFH) the frequency channel is altered at a rate which is lower than the bit rate. For example, in GSM the frequency channel is switched on a burst by burst basis. In GSM, SFH is employed for two reasons, to provide frequency diversity for slow moving mobiles and also inteferer diversity for increasing system capacity.

In order to support slow frequency hopping, it is necessary for the base station to support all time slots during the TDMA frame, consequently, the synthesiser has to frequency hop during a short period which exists between time slots, which is generally referred to as the guard period. The frequency hopping mechanism is usually accomplished by employing two Phase-Locked Loop frequency synthesisers and a single pole double throw switch. When one synthesiser is providing the transmitting frequency, the other is reprogrammed and retuned to the next. The retuning process has to be accomplished within one time slot so that the required transmitting frequency is sufficiently stable before being directed to the transmitter output. This operation is illustrated in FIG. 1, which shows the transmitting frequency allocation per time slot and the guard period.

The switching mechanism which selects the appropriate synthesiser, causes an impulsive mismatch in load impedance which pulls the synthesiser off frequency. This causes a corresponding phase disturbance inside the loop which is eventually corrected by the loop feedback mechanism. However, if the synthesiser is unable to respond quickly, then a large phase excursion can occur at the beginning of the time slot resulting in significant performance degradation.

The prior art solution to this problem is to provide an increased reverse isolation between the switch and the synthesiser. This is achieved by cascading several gain blocks interleaved with large attenuators. There are several drawbacks with the prior art solution including:

i) The wide band noise performance of the transmitter can significantly degrade,

ii) increasing the number of stages increases the component count,

iii) the power consumption of a synthesiser can increase by as much as 40%,

iv) the required synthesiser board area can increase by upto 20%.

It is desirable to have a method that would reduce the complexity and expense of the present frequency hopping schemes in time domain systems.

Summary of the Invention

According to the present invention, there is provided a method for implementing frequency hopping in a time domain system having at least a first synthesiser including the steps of locking onto a first frequency by the first synthesiser in wide loop bandwidth mode, transmitting from the first synthesiser, and converting to a narrow bandwidth mode on the first synthesiser after a delayed period of time.

In a preferred embodiment the time domain system is a TDMA system.

Brief Description of the Drawing

FIG. 1 illustrates a TDMA frame structure.

FIG. 2 illustrates power ramping employed during a guard period of the TDMA frame structure of FIG. 1.

FIG. 3 illustrates a flow chart for a preferred embodiment of the present invention.

FIG. 4 is a block diagram of a synthesiser according to the present invention.

FIG. 5 simulation results of a synthesiser according to the prior art.

FIG. 6 simulation results of a synthesiser employing the method of the present invention.

Detailed Description of the Preferred Embodiment

FIG. 1 shows a frame 2 and slot 4 structure for a time division multiple access (TDMA) system employing frequency hopping. The slots are shown changing frequency from one slot to the next thus each successive TDMA slot 4 is shown as being transmitted on a different frequency. Frequencies are changed during a guard period 6 between two slots. Two synthesisers may be employed to achieve such frequency hopping.

One synthesiser may be transmitting while a second synthesiser is tuning to the next slot's frequency. The synthesisers then switch during the guard period 6. The synthesiser that was transmitting powers down and stops transmitting and the synthesiser that was tuning powers up and starts transmitting on a new frequency. Dual loop bandwidth is employed which has independent control of both noise and switching speed.

In order to suppress the spectral emissions from the rapid switching of frequency channels, power ramping is employed during the guard period. This is illustrated FIG. 2 which shows slot n ramping down 20, 21 and slot n+1 ramping up 22, 23. The designated end of the nth time slot 20 is where the transmitting synthesiser begins ramping down and is the beginning of a guard period 20. At the end of the ramp down 21 and before the beginning of the ramp up 22 of the tuned transmitter is when the synthesisers switch from transmitting to tuning and from tuning to transmitting. The synthesiser that switches from tuning to transmitting begins ramping up 22 and ends ramp up near the start of the n+1 burst 23, the end of the guard period.

FIG. 3 shows a method according to the present invention to implement frequency hopping in a TDMA system as described. While a first synthesiser S1 is employed as the transmitting frequency as shown in step 38, a second synthesiser S2 is retuned to the next frequency in wide loop bandwidth mode as in step 30.

After a finite time period, the second synthesiser S2 locks onto a new transmit frequency and maintains wide loop bandwidth mode as in step 32.

Referring to FIG. 2 at the end of a slot time 20, the transmitter output begins to ramp down until it reaches time 21 when the transmitter output power is inhibited as described by step 40 in FIG. 3.

A finite period after ramp down 21 (FIG. 2), the second synthesiser S2 becomes the transmitting frequency as in step 34 (FIG. 3) and the first synthesiser S1 no longer transmits, step 42. At this point, the second synthesiser S2 is still in wide loop bandwidth mode.

At the end of the PA inhibit period 22 the transmitter power begins ramping up. A finite period later, the loop bandwidth converts to narrow mode operation as in step 36. In step 36, the second synthesiser S2 is in narrow loop bandwidth mode and the power ramp-up is finished. During the complete part of the active time slot and the subsequent ramp down period, the second synthesiser 2 maintains narrow loop bandwidth.

A finite period after the ramp down, the first synthesiser S1 becomes the transmitting frequency, and the second synthesiser S2 reverts back to wide loop bandwidth mode for retuning purposes.

This method is repeated and is applied to the first synthesiser S1.

Thus, a method for implementing frequency hopping is provided where a synthesiser locks onto a frequency in wide loop bandwidth mode, transmits from the first synthesiser, and then converts to a narrow bandwidth mode after a delayed period of time.

FIG. 4 shows a synthesiser circuit arrangement for implementing frequency hopping in a time domain system. The circuit arrangement permits the implementation of the above described method. It consists of two phase-locked loop synthesisers 40, 42 and a single pole double throw (SPDT) switch. Each phase-locked loop synthesiser 40 consists of four basic elements, a phase detector 44, a loop filter 46, a voltage controlled oscillator 48 and a frequency divider 45. In order to achieve both narrow and wide loop bandwidth modes of operation, the gain of the phase detector 44 is adjusted by means of the bandwidth control line 43 as illustrated in FIG. 4. The bandwidth control line 43 is a delayed version of the clock which is employed for selecting the appropriate synthesiser for the transmitting frequency. When wide loop bandwidth operation is required the bandwidth control line 43 instructs the phase detector 44 to increase its gain accordingly, which results in a corresponding increase in bandwidth. When

narrow loop bandwidth operation is required, the bandwidth control line 43 instructs the phase detector 44 to decrease its gain producing a corresponding decrease in loop bandwidth.

FIG. 5 shows the simulation results of a dual loop bandwidth synthesiser converting to narrow bandwidth before transmitting.

FIG. 6 shows the simulation results of a dual loop bandwidth synthesiser maintaining to wide bandwidth mode before transmitting and then converting to narrow bandwidth a time after transmitting according to the method of the present invention. The numbers on FIGS. 5 and 6 relate to the numbers in FIG 2.

The present invention provides an apparatus and method for implementing frequency hopping in a time domain system such as a GSM. The method of the present invention requires a synthesiser to switch to a narrow loop bandwidth mode after a finite period of time after a channel is hopped.

The benefit of the present invention is twofold. Firstly, due to the wide loop bandwidth during the guard period frequency pulling from impedance mismatches is reduced. Secondly, no additional circuitry is required for the provision of high reverse isolation between the SPDT and the VCO.

The proposed technique derives the required clock signal from the burst clock which controls the SPDT switch. This signal has to be delayed in order to provide the loop sufficient time to re-acquire lock-in. However, the delay has to be short enough to ensure suppression of phase jitter at the start of the burst, since the length of the loop impulse response will be increased. Once the loop has converted to a narrow bandwidth its impulse response remains constant during the active part of the burst and also during the power ramp down. When the output power is sufficiently small the power amplifier is inhibited to prevent spurious emissions. At this point the loop reverts back to its wide bandwidth for hopping to the next frequency channel in the next slot. This process is then repeated for the remainder and successive frames.

The present invention combines RF technology with the features of the time domain system in order to efficiently implement frequency hopping.

Claims

1. A synthesiser for implementing frequency hopping in a time domain system comprising:

means for locking onto a first frequency by the first synthesiser in wide loop bandwidth mode;

means for transmitting from the first synthesiser;

means for converting to a narrow bandwidth mode on the first synthesiser after a delayed period of time.

2. A method for implementing frequency hopping in a time domain system having at least a first synthesiser comprising the steps of:

locking onto a first frequency by the first synthesiser in wide loop bandwidth mode;

transmitting from the first synthesiser;

converting to a narrow bandwidth mode on the first synthesiser after a delayed period of time.

3. The method of claim 2 wherein the delayed period of time is defined as when a burst is transmitted from the first synthesiser.

4. The method of claim 2 wherein time domain system is a TDMA system.

5. A method for implementing frequency hopping in a time domain system substantially as herein described with reference to FIG. 3 of the drawing.

The Patent Office

Application No: GB 9424596.6 **Examiner:** Mr. Sat Satkurunath
Claims searched: 1 to 5 **Date of search:** 16 March 1995

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.N): H3A: AB, AQA, AXC,AXM; H4L: LBSF

Int Cl (Ed.6): H03L, H04L, H04J

Other: Online: WPIL, EDOC, JAPIO, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP0565127 A2	(NEC) - see especially figures 2,5 and 9	1,2,4
X	US5175511	(NEC) - see especially figure 1	1,2,4
X	US4752749	(ROCKWELL) - see especially figure 3 and column 1	1,2
X	US4568888	(TRW) - see especially figures 1 and 5	1,2
X	US4330758	(MOTOROLA) - see especially figures 3,5	1,2

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.